Dr. HARSH SOHAL
ASSISTANT PROFESSOR (SEN. GRADE)
DEPARTMENT OF ECE
JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY (JUIT)
WAKNAGHAT, SOLAN (H.P.) INDIA
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SUMMARY OF EXPERIENCE

- More than **4.5** years of research experience in biomedical system design with a focus on digital system design including DSP programming in general and FPGA system design using **VHDL** in particular, at Impedance Imaging Research Center (IIRC), **Kyng Hee University, South Korea**.
- More than **8** years of teaching experience at undergraduate and post graduate level in government and private universities in India.
- **11** months industrial research experience as Engineer R & D in Recorders & Medicare Systems Pvt. Ltd (RMS), Chandigarh, India.

EDUCATIONAL QUALIFICATION

Course	Board/University	Year of passing
Ph. D. (Biomedical Engineering)	College of Electronics and Information, Kyung Hee University, South Korea	2014
M.Tech. Electronics (VLSI Design)	NIT, Hamirpur, India	2008
B.Tech. (Electronics & Instrumentation Engineering)	Punjab Technical University, Jalandhar, India	2005

RESEARCH EXPERIENCE

September, 2009 –March, 2014: Research Assistant in Impedance Imaging Research Center, Kyung Hee University, South Korea.
Employer: Prof. Eung Je Woo, Director IIRC, Kyung Hee University, South Korea.
Duties and responsibilities: DSP programming, FPGA specification design, programming using VHDL, implementation, simulation, verification, system testing and debug, including integration of hardware/software components to demonstrate the complete working system**.**

PROJECTS UNDERTAKEN:

The FPGA specification, design, development, test and debug along with DSP programming have been done for:

- Bio-impedance Spectroscopy System
- Trans Admittance Mammography system
- EIT KHU Mk 2.5 (16 channel, 32 channel)
- Cascaded KHU Mk 2.5 (Implemented IEEE 1588,clock synchronization)
- EEG EIT integrated system

TEACHING EXPERIENCE (8 YEARS+)

- **March 27, 2017 –till date: Assistant Professor (Sr. Grade) (ECE)**

University / Institute: Jaypee University of Information Technology Waknaghat, Distt. Solan, (H.P.), India

- **Jan 05, 2015 – March, 2017: Assistant Director | Research**
  University / Institute: Chitkara University, Punjab, India.

- **July 21, 2014 – Dec 15, 2014: Assistant Professor(Contract)**
  University / Institute: Electronics and Communication Engineering Department, National Institute of Technology (NIT) Jalandhar, Punjab, India.

- **August 01, 2008 – July 21, 2009: Lecturer**
  University / Institute: Electronics and Communication Engineering Department, National Institute of Technology (NIT) Hamirpur, Himachal Pradesh, India.

INDUSTRY EXPERIENCE

August 29, 2005 – July 22, 2006: Engineer (R&D) trainee.

Company: Recorders & Medicare Systems Pvt. Ltd (RMS), Chandigarh, India
Duties and responsibilities: I was involved in the project of EEG dipole localization. As *Engineer (R&D) trainee* I worked as a software programmer in visual C++ to acquire the data from hardware to display the acquired data on the monitor. I was also given the experience of testing and debugging the assembled circuit board by using the designed schematics and layouts. As *Engineer (R&D)* my job was to work together with a team of software programmers to search, understand and implement the algorithms to show the dipole localization in 3D human head model. I primarily worked on selecting the related research papers and algorithms to explain and discuss with other team members whose main focus was on implementation.

ADMINISTRATIVE EXPERIENCE:

1. Hostel Warden from January 2018 to Feb 2021.
2. Member of examination committee since October 24, 2019.
3. B. Tech project coordinator (1.5 years)
4. Conference Secretary IEEE ISPCC-2k21
5. Member, University Admission Cell (2021-2022)

TECHNICAL SKILLS:

Programming Languages:	HDLs (Verilog and VHDL) abd C, C++.
Programming Tools:	MATLAB, LAB View.
VLSI Design Tools:	Knowledge of standard EDA tools such as Quartus IIAltera (Currently working with), T-Spice, S-Edit, L-Edit, Xilinx 9.2i, Modelsim,CadenceTools, MentorGraphic Tools, Eldo.
Others:	MS Office, Latex, COMSOL

JOURNAL PUBLICATIONS:

1. Youssoufa Mohamadou, Tong In Oh, Hun Wi, Harsh Sohal, Adnan Farooq, Eung Je Woo and Alistair Lee McEwan, "Performance evaluation of wideband bio-impedance spectroscopy using constant voltage source and constant current source", *Measurement Science and Technology*,volume 23, number 10, Sep. 2012. *(SCI IF: 1.861)*
   Online ISSN: 1361-6501 Print ISSN: 0957-0233
2. Wi, H, Sohal, H. ; McEwan, A.L. ; Woo, E.J. ; Oh, T.I., "Multi-Frequency Electrical Impedance Tomography System With Automatic Self-Calibration for Long-Term Monitoring", *Biomedical Circuits and Systems, IEEE Transactions on*,Volume: 8, Issue: 1, Feb. 2014, pp:119 – 128. Print ISSN: 1932-4545 Electronic ISSN: 1940-9990 (*SCIE IF: 4.252)*)

3. Kumar N, Sohal H, "Impact of Various Weather Condition on the Performance of Free Space Optical Communication System",*Journal of Optical Communications*, Volume 35, Issue 1, Pages 45–49, ISSN (Online) 2191-6322, ISSN (Print) 0173-4911, DOI: 10.1515/joc-2013-0060, January 2014. (SCOPUS Indexed)
4. Harsh Sohal, Hun Wi, Alistair Lee McEwan, Eung Je Woo and Tong In Oh, "Electrical Impedance Imaging System based on FPGAs to enable Flexibility and Interoperability", *Biomedical Engineering Online*, **13**:126, August 30,2014. *ISSN: 1475-925X (electronic) (SCIE IF: 2.013)*
5. Eun Jung Lee, Hun Wi, Alistair Lee McEwan, Adnan Farooq, Harsh Sohal, Eung Je Woo, Jin KeunSeo and Tong In Oh, "Design of microscopic electrical impedance tomography system for 3D continuous non-destructive monitoring of tissue culture", *Biomedical Engineering Online*, **13**:142 , October 06, 2014 ISSN: 1475-925X (electronic).
(SCIE IF: 2.013)
6. Sangha S. H., Sohal H., "Power Challenges in Wireless Body Area Network for Mobile Health Powered by Human Energy Harvesting: A Survey", *Indian Journal of Science and Technology*, Volume 9, Number 46, Dec. 2016. Print ISSN : 0974-6846; Online ISSN : 0974-5645
(SCOPUS Indexed)
7. Kaur H., Kaur A., Sohal H., Gupta I., Singh. S.,Nagpal S., "Design and Performance Analysis of RAM_WR_Control Module using Xilinx ISE 14.2", *Indian Journal of Science and Technology*, Volume 9, Number 46, Dec. 2016. Print ISSN : 0974-6846;Online ISSN : 0974-5645 (SCOPUS Indexed)
8. Sharma A., Sohal H., "Considerations for Ultra Low Power VLSI Design – A Survey", Journal *of Nanoelectronics and Optoelectronics*, Volume 12, Number 1, Jan. 2017, pp. 1-21(21). ISSN: 1555-130X (Print): EISSN: 1555-1318 (Online) *(SCIE IF: 1.069)*
9. Garima Thakur, Harsh Sohal, Shruti Jain (2018). Design and Comparative Performance Analysis of various Multiplier Circuits. *Journal of Scientific and Engineering Research, 5* (7), 340-349. ISSN: 23942630
10. Garima Thakur, Harsh Sohal, Shruti Jain (2018). High Speed Radix-2 Butterfly Structure using Novel Wallace Multiplier. *International Journal of Engineering and Technology (UAE), 7* (3), 213-217. ISSN: 2227-524X
11. Garima Thakur, Harsh Sohal, Shruti Jain (2018). An Efficient Design of 8-bit High Speed Parallel Prefix Adder. *Research Journal of Science and Technology, 10* (2), 105-114. ISSN (ONLINE): 2349-2988 ISSN (PRINT) : 0975-4393
12. Kirti, Harsh Sohal, Shruti Jain (2018). Comparative Analysis of Heart Rate Variability Parameters for Arrhythmia and Atrial Fibrillation using ANOVA. *Biomedical and Pharmacology Journal*, 11 (4), 1841-1849. ISSN: 0974-6242; e- ISSN: 2456–2610
(SCOPUS Indexed)
13. Harsh Sohal, Bishal Karki, Anjali Sharma,Yousouffa Mohamadou (2018). Design of impedance measurement module for an eeg and eit integrated system. International Journal of Control and Automation, 11 (9), 97-108. ISSN: 2005-4297 (SCOPUS Indexed)
14. Anjali Sharma, Harsh Sohal, Harsimran Jit Kaur (2019). Sleepy CMOS-Sleepy Stack (SC-SS): A Novel High Speed, Area and Power Efficient Technique for VLSI Circuit Design. *Journal of Circuits, Systems and Computers*, 28 (11), 1950197-1950222. ISSN (print): 0218-1266 | ISSN (online): 1793-6454 *(SCIE IF 0.595)*
15. Kirti, Harsh Sohal, Shruti Jain (2019). FPGA implementation of Power-Efficient ECG pre-processing block. *International Journal of Recent Technology and Engineering*, 8 (1), 2899-2904. ISSN: 2277-3878 (Online) (SCOPUS Indexed)
16. Anjali Sharma, Harsh Sohal (2019). Sleepy-Gate Diffusion Input (S-GDI) Ultra Low Power Technique for Digital Design . International Journal of Innovative Technology and Exploring Engineering (IJITEE), 9 (1), 4340-4347. ISSN: 2278-3075 (Online) (SCOPUS Indexed)
17. Kirti, Harsh Sohal, Shruti Jain (2020). Multistage Classification of Arrhythmia and Atrial Fibrillation on Long- Term Heart Rate Variability. *Journal of Engineering Science and Technology, 15* (2), 1277-1295. (SCOPUS Indexed)

18. Kirti, Harsh Sohal, Shruti Jain (2020). Computer Aided Diagnostic System for Feature Based Classification using Heart Rate Variability. *Biomedical Engineering Applications, Basis and Communications, 32* (2).

19. Kirti, Harsh Sohal, Shruti Jain (2020). Design and Implementation of Low Power ECG Pre-processing Module on Xilinx FPGA. *IETE Journal of Research, Online* (15 Mar 2020). DOI: 10.1080/03772063.2020.1725660 *(SCIE IF: 2.225)*

20. Kirti, Harsh Sohal, Shruti Jain (2020). Statistical Analysis of HRV Parameters for the Detection of Arrhythmia. International Journal of Image and Graphics, 20 (4).
21. Garima Thakur, Harsh Sohal, Shruti Jain (2021). A novel parallel prefix adder for optimized Radix 2 FFT processor. Multidimensional Systems and Signal Processing, 32, pages 1041–1063. *(SCI/SCIE IF: 2.030)*
22. Garima Thakur, Harsh Sohal, Shruti Jain (2021). A Novel ASIC-Based Variable Latency Speculative Parallel Prefix Adder for Image Processing Application. Circuits, Systems and Signal Processing, 40, pages 5682–5704. Published: 17 May 2021. *(SCIE IF: 2.225)*
23. Kirti, Harsh Sohal, Shruti Jain (2022). FPGA implementation of collateral and sequence pre-processing modules for low power ECG denoising module. Informatics in Medicine Unlocked, 28 (100838)

INTERNATIONAL CONFERENCE PUBLICATION/PRESENTATION

1. Sohal H, Wi H, Oh T I, and Woo E J, Design of impedance measurement module for an EEG and EIT integrated system, in Proceedings of 13th International Conference on Biomedical Applications of Electrical Impedance Tomography, May 23-25, 2012, Tianjin, China.
2. Sohal H., Design and Simulation of CMOS Inverter Based Fully Digital Flash ADC for Biomedical Applications, 4th Edition of International Conference on Wireless Networks and Embedded Systems WECON-2015, March 20-21, 2015, Chitkara University, Punjab, India.
3. Kaur H., Sohal H. and Singh J., Design and performance analysis of UART using Altera Quartus-II and Xilinx ISE 14.2, 6th Edition of International Conference on Communication Systems and Network Technologies, CSNT-2016, March 05-07, Chitkara University, Punjab, India.
4. Sharma A., Sohal H., Area-Power Efficient 4- Bit Signed Adder Design for Arithmetic Applications, 6th Edition of International Conference on Communication Systems and Network Technologies, CSNT-2016, March 05-07, Chitkara University, Punjab, India.
5. Garg D., Sohal H., and Ahuja S., SSTL IO standard based power efficient data processing device design on FPGA, 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), March 18-19, 2016, Noorul Islam Center for Higher Education, Tamilnadu, India.
   (Published in IEEE Xplore. DOI: 10.1109/ICCPCT.2016.7530268)
6. Sharma A.,Sohal H., Sharma K, Area and Power Analysis of Adiabatic 2x1Multiplexer Design on 65nm CMOS Technology, 5th Edition of International Conference on Wireless Networks and Embedded Systems, IEEE WECON-2016, October 15-16, Chitkara University, Punjab, India.
   (Published in IEEE Xplore. DOI: 10.1109/WECON.2016.7993489)
7. Kaur H. Aggarwal D., Singh S.,Tandon P., Thaku C., Sohal H., Sharma K, Area and Power Analysis of Adiabatic 2x1Multiplexer Design on 65nm CMOS Technology, 5th Edition of International Conference on Wireless Networks and Embedded Systems, IEEE WECON-2016, October 15-16, Chitkara University, Punjab, India.
   (Published in IEEE Xplore. **DOI:** 10.1109/WECON.2016.7993476)
8. Kirti, Sohal, H., Jain, S., Interpretation of Cardio Vascular Diseases using Electrocardiogram: A Study, IEEE 5th International Conference on Parallel, Distributed and Grid Computing (PDGC-2018), 20-22 Dec, 2018, Solan, India.
9. Garima Thakur, Harsh Sohal, Shruti Jain (2020). Design and Analysis of High-Speed Parallel Prefix Adder for Digital Circuit Design Applications. Proceedings of the International Conference on Computational Performance Evaluation (ComPE) [North - Eastern Hill

University, Shillong, Meghalaya, India : Jul 2-4, 2020]

10. Garima Thakur, Harsh Sohal, Shruti Jain (2021). Implementation of Approximate Multiplier using Inexact Compressors. Proceedings of the 6th International Conference on Signal Processing, Computing and Control [JUIT Waknagha (H.P.): October 07-09, 2021], pp.165-170.
11. Himani, Shruti Jain, Harsh Sohal (2021). Design of Global Interconnects using Adiabatic Dynamic Logic employing FinFET Technology. Proceedings of the 6th International Conference on Signal Processing, Computing and Control [JUIT Wakaghat (H.P.): October 07-09, 2021], pp.450-455.

BOOKS/ BOOK CHAPTERS:

1. Rajiv Kumar, Shruti Jain, Harsh Sohal (2021). Signal Processing, Computing and Control (6th). USA: IEEE. [ISBN : 978-1-6654-2554- 4]
2. Kirti, Harsh Sohal, Shruti Jain (2022). FPGA Implementation of Low Power Pre-processor Design for Biomedical Signal Processing Application. In Rao V.V., Kumaraswamy A., Kalra S., Saxena A., Computational and Experimental Methods in Mechanical Engineering. Smart Innovation, Systems and Technologies (pp. 489-497). : Springer. [ISBN: 978-981-16-2857-3-48]

NATIONAL CONFERENCE PUBLICATION

1. Philemon Daniel, Janamani Chandram Ayyangalam, Harsh Sohal, “Testing of SOCs- A Fresh Perspective” in National Conference on “Design Techniques for Modern Electronic Devices, VLSI and Communication Systems, DTVC-2007”, held at NIT Hamirpur, Himachal Pradesh.

PATENTS & COPYRIGHTS:

- Filed a patent titled "IMPROVED LIGHT SPOT GALVANOMETER", vide patent filing number: 3773/DEL/2015, dated 18/11/2015. **(Granted Patent No. 382409)**
- Filed a patent titled "WIRELESS COMMUNICATION DEVICE FOR IMPROVED WIFI SIGNAL" vide patent filing number: 3888/DEL/2015, dated 28/11/2015
- Filed a patent titled “MOBILE PHONE WITH A MECHANISM TO LOCK POWER BUTTON FOR PREVENTING THE UNAUTHORIZED USE", vide patent filing number: 201611022659, dated 01/07/2016.
- Filed a patent titled “ELECTRONIC ASSISTIVE DEVICE FOR CLASSROOM TEACHING", vide patent filing number: 201611031193, dated 13/09/2016.
- Filed a patent titled “ADVANCED AUTONOMOUS WALL PAINTING MACHINE FOR HIGH RISE BUILDINGS", vide patent filing number: 201711003499, dated 31/01/2017.

AWARDS/SCHOLASHIPS

- Proposal entitled, “Electrochemical storage of hydrogen in activated charcoal”, of which I am a Co-PI, is selected in top 5 proposals in Elsevier Foundation Green and Sustainable Chemistry Challenge 2017.
  The team members include:-
  Dr. Amandeep Singh Oberoi, CURIN, Chitkara University
  Dr. K R Ramkumar, CURIN, Chitkara University
  Dr. Pankaj Kumar, CURIN, Chitkara University
  Dr. Harsh Sohal, CURIN, Chitkara University
  Dr. Tapas Kuila, CSIR-Laboratory of Mechanical Engineering, Durgapur
  http://www.greensuschemconf.com/green-chemistry-challenge.asp
- Presidential Graduate Student Scholarship, Kyung Hee University, South Korea (2009 – 2011).
- Graduate Research Assistantship, Impedance Imaging Research Center, Department of Biomedical Engineering, Kyung Hee University, South Korea (2009 – 2014).
- Meritorious Student Scholarship, covering tuition, boarding and lodging expenses, Ministry of Human Resources and Development, Government of India (1993-2000).

RESEARCH GUIDANCE:

- Ph. D. (Joint Guidance)
  - Completed (02)
  - Under guidance (02)
- Ph. D. (Sole Guidance)
  - Under guidance (01)
- M. Tech. (Joint Guidance)
  - Completed (05)

MEMBERSHIP OF PROFESSIONAL BODIES:

- IEEE Sr. Member
- Life member Biomedical Engineering Society of India (BMESI)
- Member International Association of Engineers (IAENG)

Orientation/Refresher Courses, Summer/Winter Schools, Faculty Development Programmes, Seminars/Conferences/Workshops Attended/ Organized:

S. No.	Title	Dates/ Duration	Sponsoring Agency and Organisation & Place held	Attended/Organized
1	12 week FDP on "Problem Solving through Programming in C"	Spt- Dec 2020	NPTEL – AICTE	Attended
2	Advanced Optimization Techniques and hands-on with MATLAB/SCILAB	13 – 24 July 2020	Electronics and ICT Academies held from & MeitY	Attended
3	Organized a conference on, "Technologies for Environment stability and smart Agriculture"	Set 18-19, 2020 (Two Days)	JUIT	Organized
4.	Webinar on Issues and Trends in Contemporary Indian Education by Ms. Krittika Tewari	8th Aug 2020	Online, ECE Dept, JUIT	Organized
5	Vicharana-2020, 17th Oct 2020	17th Oct 2020	ECE & TIEDC, JUIT	Organized (
6	Vicharana 2.0: Toy Innovation Challenge, 16th Jan 2021	16th Jan 2021	ECE & TIEDC, JUIT	Organized
7	Webinar on Design Thinking for Innovation" by Ms.Tarunam Mahajan	21st Aug 2020	Online, ECE Dept, JUIT	Organized
8	Webinar on Interdisciplinary approaches to improve resiliency at scales for humans and ecosystems to thrive by Dr. Ashish Sharma	29th Aug 2020	Online, ECE Dept, JUIT	Organized
9	Webinar on An introduction to AR-VR (Augmented Reality-Virtual Reality) and the way its transforming the world we live in by Mr. Sanjay Singh	5th Sep 2020	Online, ECE Dept, JUIT	Organized
10	Webinar on Telecom Technologies, their evolution and RF optimization of KPIs by Mr. Gaurav Joshi	19th Sep 2020	Online, ECE Dept, JUIT	Organized
11	Webinar on Advanced Driver Assistance Systems (ADAS) by Mr. Shubhender Singh	3rd Oct 2020	Online, ECE Dept, JUIT	Organized
12	Webinar on Edge Computing by Ms. Aastha Afsar	10th Oct 2020	Online, ECE Dept, JUIT	Organized

13	Webinar on Analysis and Classification of Breast Abnormalities using Ultrasound Images by Dr. Kriti	24th Oct 2020	Online, ECE Dept, JUIT	Organized
14	FDP in R Programming	28th April, 2020 to 2nd May, 2020	National Mission on Education through ICT, MHRD, Govt. of India	Attended
15	One week STC on Artificial Neural Networks and Fuzzy Logic through ICT	23-27, July. 2018	NITTTR, Chandigarh. JUIT Waknaghat	Attended
16	One week FDP on Recent Trends on Machine Learning for Signal Processing (RTMLS)	20-25, May, 2019	JUIT, Waknaghat	Attended
17	Organized an invited talk on HDL Based System Design	April 15, 2019	JUIT, Waknaghat	Organized
18	4th IEEE International Conference on Signal Processing, Computing & Control (ISPCC 2017)	Sept 21-23, 2017	IEEE, JUITW Waknaghat	Organized; member organizing committee
19	National symposium on medical image acquisition	Nov 20-22, 2017	AIIMS delhi; JUITW	Attended
20	Workshop on Massive Open Online Courses (MOOCS)	Sept 15, 2017	NPTEL, Computer Society of India	Attended
21	One day workshop on Patent Drafting	Oct 13, 2017	HIMCOSTE; JUIT Waknaghat	Attended
22	Short term course on Wireless and Mobile Communication through ICT	Oct 30 to Nov 3, 2017 (One Week)		Attended

Special/ Extension/ Expert/Invited Lectures Delivered:

1. Delivered Expert Lecture in a One-Day Workshop on "Technology & Society" organized by Faculty Development Centre - SMVDU under Pandit Madan Mohan Malviya National Mission on Teachers and Teaching (PMMMNMTT) Scheme in the Online Mode (September 24, 2021)
2. Delivered an expert lecture in Online Short Term Course on Recent Advances in Computational Intelligence for Signal Processing (RACISP-2020) Organized by the Department of ECE, JUIT
3. Delivered an expert lecture titled, "Introduction to FPGA based Signal Processing", in Atal Bihari Government Institute of Engineering & Technology, Pragatinagar, Shimla (H.P.), in Online Mode on October 16, 2020.

Contribution/ Participation in Departmental Activities & Development:

1) DPMC member in ECE Department
2) Faculty Incharge of CL1 Lab
3) Department Club Coordinator (Technovators)
4) Mock Interview committee member
5) Modernization and up gradation of Lab Committee member
6) Co-Coordinator e Yantra Lab
7) Student Feedback coordinator

8) Student mentoring
9) Engaged courses during winter vacation
10) Evaluation of Projects of Final and third years students

Contribution/ Participation in Institute Activities & Development:

1) Hostel Warden, H1 & H6
2) Member Admission Cell of the University
3) DPMC member CSE Department (4 scholars)
4) Member Centre of Excellence for Sustainable Technologies for Rural Development(CESTRD)
5) Member Examination Committee
6) Member Anti ragging squad
7) Covid-19 safety norms implementation committee member
8) Member of Group-5 Created for All Jaypee Group Universities
9) Member Disciplinary Committee (Feb 05, 2021)
10) Member- review and mentorship TIEDC cell