ADVANCED CMOS DIGITAL DESIGN TECHNIQUES

(Core/ Elective Subject)

Course Code:	14M1WEC231	**Semester:**	2nd Semester, M.Tech (ECE) and 8th Semester, B. Tech (ECE)
Credits:	3	**Contact Hours:**	L-3, T-0, P-0

Course Objectives

1. To study advanced concepts of CMOS Digital Design. It will be helpful for the students when they work in VLSI industries or in R&D's.
2. To cover crucial real world system design issues such as signal integrity, power dissipation, interconnect packaging, timing and synchronization.
3. To provide unique coverage of the latest design methodologies and tools.
4. To learn Low-power design concepts and voltage-frequency scaling.

Course Outcomes

This course provides the knowledge of Advanced CMOS Digital Design Techniques. After study through lectures and assignments, students will be able to do the

1. Modeling and estimation of R, C, and L parasitics, effect of technology scaling, sheet resistance, techniques to cope with ohmic drop and capacitive cross talk, estimating RC delay, and inductive effects.
2. Several lab team assignments to design actual VLSI subsystems from high level specifications, culminating in a course project involving the software design of a modest complexity chip.
3. Several homework assignments based on core concepts and reinforcing analytical skills learned in class.

Course Contents

Unit	**Topics**	**References (chapter number, page no. etc)**	**Lectures**
1.	Introduction, The Wire, Coping with Interconnect: Impact of Interconnect Parasitic, Impact of Resistance, Impact of Capacitance, Cross-talk, Reducing RC-delay, Dealing with inductance.	Rabaey (Page 135-148, 445- 475)	5
2.	Designing Sequential Logic Circuits: Self Timed Circuit Design, Self Timed Signaling, Muller-C Element, Two Phase Handshake Protocol, Self Resetting CMOS, Synchronizer, Designing Latch and Edge triggered Register using different approach, Clock Overlaps, C2MOS Logic, TSPC Logic, Specialized edge triggered TSPCR, Pulse Registers, Pipelining, Designing Schmitt Trigger and multi-vibrators, Design Techniques for large Fan in, Sizing	Rabaey (Chapter 10.4, 10.5, Chapter 7) Rabaey Page (261-273)	16

	combinational circuits for minimum delay, Ratioed Logic: DCVSL, Pass transistor Logic, Differential Pass transistor Logic.		
3	Arithmetic Circuits: Adders (Ripple-Carry Adder, Complimentary Static CMOS FullAdder, Mirror Adder, Transmission Gate Full Adder, Carry-Bypass Adder, Carry-Select Adder, Logarithmic Look-Ahead Adder, Tree Adders). Multipliers (Array Multiplier, Wallace-Tree Multiplier, Booths Multiplier Algo), Shifters (Barrel Shifter, Logarithmic Shifter).	Rabaey (Chapter 11) Uyemura (Chapter 12)	11
4	Semiconductor Memories: Memory Timing, Memory Architecture, Read-Only Memory Cells, MOS OR ROM, MOS NOR ROM, MOS NAND ROM, Dual Data rate Synchronous Dynamic RAM, DRAM Timing, Sources of Power Dissipation in Memories, Data Retention in SRAM, Suppressing Leakage in SRAM, Data Retention in DRAM.	Rabaey (Chapter 12)	9
		Total Number of Lectures	**41**

Evaluation Scheme

1. Test 1 : 15 marks
2. Test 2 : 25 marks
3. Test 3 : 35 marks
4. **Internal Assessment** : 25 marks
   - 10 Marks : Class performance, Tutorials & Assignments
   - 10 Marks : Quizzes
   - 5 marks : Attendance

Text Books

1. J. Rabaey, A. Chandrakasan; "Digital Integrated Circuits: A Design Perspective", 3rd and B. Nikolic Edition 2003.
2. John P. Uyemura;"Introduction to VLSI Circuits and Systems", John Wiley & Sons, Inc, 2002.

Reference Books

1. Sung-Mo Kang, Yusuf Leblebici,: CMOS Digital Integrated Circuits Analysis and Design",Tata McGraw-Hill Edition 2003

Web Resources

1. URL1:- http://nptel.ac.in/courses/117106092/
2. URL2:- http://nptel.ac.in/courses/117106093/