ECE DESIGN AND SIMULATION LAB-1

(Core Subject)

Course Code:	10M17EC171	Semester:	1 st Semester, M. Tech. (ECE)
Credits:	2	Contact Hours:	L-0, T-0,P-2

Course Objectives

The objectives are to study:

- 1. The steps involved in the designing and simulation of a communication system.
- 2. To know how to design model for a digital electronic circuit.

Course Outcome

- 1. To equip with engineering skills by way of breadboard circuit design with electronic devices and components.
- 2. Have confidence in designing an electronic circuit from scratch and able to demonstrate the practical aspects of basic electronics theory.
- 3. Simulate and test the Analog, Digital and mixed Electronics circuits using OrCAD/PSPICE software.

List of Experiments

- 1. Introduction to MATLAB programming.
- 2. To generate Amplitude modulated signal:
 - i) To observe an under-modulated signal.
 - ii) To observe a perfect modulated signal.
 - iii) To observe an over modulated signal.
- 3. To generate a Frequency modulated signal:
 - i) Vary the frequency deviation and observe the changes in modulated wave.
- 4. To generate a Pulse code modulated signal.
- 5. To study Huffman Coding.
- 6. To generate a Binary phase shift keying signal.
- 7. To make a project in MATLAB.
- 8. Introduction to XILINX Programming.
- 9. To write a Verilog HDL programme for half adder.

- 10. To write a Verilog HDL programme for full adder.
- 11. To write a Verilog HDL programme for full adder using half adders.
- 12. To write a Verilog HDL programme for 2:1 multiplexer and 4:1 multiplexer.
- 13. To write a Verilog HDL programme for 4:1 multiplexer where the inputs and output are 8 bits.
- 14. To write a Verilog HDL programme for 4 bit binary numbers addition and subtraction using conditional statement.
- 15. To make a project in Verilog HDL.

Evaluation Scheme

1.	Mid Sem Evaluation	20 Marks
2.	End Sem Evaluation	20 Marks
3.	Attendance	15 Marks
4.	Class response	30 Marks
5.	File	15 Marks

Total Marks 100 Marks

Text Books

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Second Edition, Prentice Hall PTR (2003).