VLSI LAB

(Core Subject)

Course Code:	10B17EC672	**Semester:**	6th Semester, B. Tech (ECE)
Credits:	1	**Contact Hours:**	L-0, T-0,P-2

Course Objectives

1. To study the constructs, conventions and design capabilities of the Verilog HDL
2. To study gate level , dataflow (RTL), behavioral, and switch level modeling, describes leading logic synthesis methodologies
3. To use the xilinx platform to write test benches and simulate the digital system designs
4. To learn to implement a given algorithm into an FPGA breaking it into modules and sub modules

Course Learning Outcomes

After studying this course the students shall be able to:

1. Apply the techniques of design, simulation and synthesis of digital circuits to design FPGA based systems or/and ASICs using Xilinx design tools
2. Explain and design the test benches for verification of the given IP core or HDL based design.
3. Able to explain the System Modeling with Tasks and Functions
4. Design digital circuits for implementing a signal processing algorithm using different verilog modelling styles.

List of Experiments

1. Learn how to use of XILINX ISE simulator by writing the Verilog code to simulate a half adder; where a, b are 1-bit input
2. Write data flow Verilog HDL model for Half Adder using different modelling technique
3. Write data flow Verilog HDL model for Full Adder
4. Using strutural modeling of Verilog HDL perform the following:
   - Half adder with proper test stimulus.
   - Full adder (using half adder module of part 1) with proper test stimulus
5. Write down Verilog HDL code of the following
   - Data flow model of 2x1 Multiplexer with proper test stimulus.
   - Structural model of 2x1 Multiplexer with proper test stimulus.
6. Write the hardware description of a 4:1 multiplexer
   - Using behavioural modelling
   - Using structural modelling
   - Using 2:1 multiplexer

7. Write down Verilog HDL code of 2x1 Multiplexer and 4x1 Multiplexer using **if-else** statement, **case** statement and **ternary** operator.
8. Write the hardware description of a 2:1 multiplexer and 4:1 multiplexer , each input and output of this multiplexer is of 4-bit.

```
module mux (a,b,sel,result);
input [3:0] a,b;
input sel;
output [3:0] result;
.....
endmodule
```

9. Write the hardware description of a 4-bit adder/Subtractor
10. Write data flow Verilog HDL model for Encoder/ Decoder using any modelling technique
11. Simulate the Verilog HDL code for the following
    - D-Latch using proper test stimulus.
    - D-flip flop using proper test stimulus.
12. Write the Verilog HDL code for a JK Flip flop, and its test-bench.
13. Write the hardware description of a 8-bit register with shift left and shift right modes of operation
14. Write the Verilog HDL code of a 4-bit PRBS (pseudo-random Binary sequene) generator using a linear feed-back shift register and test it. Choose your own polynomial for the generator.

Evaluation Scheme

1. Mid Sem Evaluation	20 Marks
2. End Sem Evaluation	20 Marks
3. Attendance	15 Marks
4. Class response	30 Marks
5. File	15 Marks
Total Marks	**100 Marks**

Text Books

1. John P. Uyemura: Introduction to VLSI Circuits and Systems, John Wiley & Sons, , Inc, 2002
2. Samir Palnitkar, “Verilog HDL”, Pearson Education (2nd edition)