DIGITAL ELECTRONICS LAB

(Core Subject)

Course Code:	10B17EC407	Semester:	3rd Semester B.Tech. (CSE and IT) 4th Semester, B. Tech. (ECE)
Credits:	1	Contact Hours:	L-0, T-0, P-2

Course Objectives

The objectives are to study

1. To provide students basic experimental experiences in constructing digital circuits, measuring the experimental data and analysis of the results.
2. To develop skills to design various combinational and sequential circuits using electronics devices.

Course Outcomes

After studying this course the students would gain enough knowledge.

1. To acquire knowledge about electronic components and hardware devices required for designing digital electronics circuits.
2. Foster ability to identify, analyze and design combinational circuits.
3. Foster ability to design various synchronous and asynchronous sequential circuits.
4. To acquire knowledge about internal circuitry and logic behind any digital system.
5. To develop skill to build, and troubleshoot digital circuits.

List of Experiments

Introduction (About Bread Board)

1. To implement Logic gates using TTL ICs (7400, 7402, 7404, 7408, 7410, 7411, 7420, 7427, 7432, 7486).
2. Implementation of Combinational Circuits.
3. To verify NAND and NOR gates are universal gates.
4. Implementation of Combinational Logic Design using 74** ICs.
5. Simplification of Boolean expression using Karnaugh Map Method.
6. To design a 4 bit Binary to Gray code Converter, bit Gray to Binary code Converter, 3 bit Binary to Excess-3 code Converter.
7. To implement Adder and Subtractor circuits:- (Half and Full using simple gates and universal gates).
8. Implement multiplexer using gates and TTL IC's.
9. To verify the truth table of Binary (2 bit) to decimal decoder and octal to decimal decoder.

10. To verify the truth table of one bit and two bit Comparators using logic Gates.

11. To verify the truth tables for each (a) DDL OR gate (b) DDL AND gate (c) TTL OR gate (d) TTL AND gate (e) TTL NAND gate (f) TTL NOR gate.

12. Functional table verification of Latches:-

(i) SR-Latch with NOR Gates

(ii) SR-Latch with NAND Gates

(iii) SR-Latch with control input using NAND Gates

(iv) D Latch

(v) T Latch

Evaluation Scheme

1. Mid Sem Evaluation	20 Marks
2. End Sem Evaluation	20 Marks
3. Attendance	15 Marks
4. Class response	30 Marks
5. File	15 Marks
Total Marks	**100 Marks**

Text Books

1. Thomas L Floyd "Digital Fundamentals"