

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

One Week Hands-on Workshop on

“VLSI Design”

March 04-09, 2024



**One-week Hands-on Workshop on “VLSI Design”
(04th - 09th March, 2024)**
organized by
**Department of Electronics & Communication Engineering,
Jaypee University of Information Technology**
in collaboration with
**Department of Technical Education, Vocational & Industrial Training,
Government of Himachal Pradesh**



In a significant stride towards advancing knowledge in the field of VLSI Design, Jaypee University of Information Technology (JUIT), Wagnaghat, organized a one week hands-on workshop on “VLSI Design”. This workshop, a collaborative effort between JUIT’s Department of Electronics and Communication Engineering and the Department of Technical Education, Vocational, and Industrial Training, Government of Himachal Pradesh and

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

Institution's Innovation Council (IIC), commenced on March 04, 2024, and continued until March 09, 2024. The event witnessed active participation from over 75 enthusiasts hailing from various districts of Himachal Pradesh.



The poster is for a "One-week Hands-on Workshop on 'VLSI Design'" held from 04th to 09th March, 2024. It is organized by the Department of Technical Education, Vocational & Industrial Training, Government of Himachal Pradesh, in collaboration with Jaypee University of Information Technology, Department of Electronics & Communication Engineering. The poster lists the Patron (Prof. R.K. Sharma), Advisor (Prof. Ashok Kumar Gupta), Program Chair (Prof. P.B. Barman), Finance Chair (Maj. Gen Rakesh Bassi), Convener (Prof. Shruti Jain), and Coordinators (Dr. Harsh Sohal, Prof. (Asso.), ECE and Dr. Pardeep Garg, Prof. (Asst.), ECE). It also lists Resource Persons including Dr. Harpreet Singh Jatana, Dr. Balwinder Singh, Dr. Balwinder Raj, Dr. Satish Chandra Tiwari, Mr. Mayank Singh, Mr. Ankur Sangal, and Mr. Anish K Sharma. The poster includes an "About Jaypee University of Information Technology" section, an "About Department of Technical Education, Vocational and Industrial Training" section, and an "Objective of the Workshop" section. It also provides contact information for Dr. Pardeep Garg and Dr. Harsh Sohal, and a registration link: <http://tinyurl.com/juitecevlsi>. The bottom right of the poster features an aerial view of the Jaypee University campus.

Patron
Prof. R.K. Sharma, Vice Chancellor

Advisor
Prof. Ashok Kumar Gupta,
Dean (Academics & Research)

Program Chair
Prof. P.B. Barman, Head, PMS Department
Prof. Rajiv Kumar, Head, ECE Department

Finance Chair
Maj. Gen Rakesh Bassi (Retd.),
Registrar and Dean of Students

Convener
Prof. Shruti Jain, Associate Dean
(Innovation) and Prof. ECE

Coordinators
Dr. Harsh Sohal, Prof. (Asso.), ECE
Dr. Pardeep Garg, Prof. (Asst.), ECE

Resource Persons

- Dr. Harpreet Singh Jatana, Former group head at SCL Mohali and ISRO.
- Dr. Balwinder Singh, Joint Director & Head, ACS Division, CDAC Mohali.
- Dr. Balwinder Raj, Professor (Asso.), NIT Jalandhar.
- Dr. Satish Chandra Tiwari, DFT Manager (Principal Design Engineer), NXP Semiconductors.
- Mr. Mayank Singh, Verification Engineer, NXP Semiconductors.
- Mr. Ankur Sangal, Technical Lead, HCL Technologies.
- Mr. Anish K Sharma, Entuple Technologies Pvt. Ltd. Bangalore.

Contact:
Dr. Pardeep Garg,
8894329649, pardeep.garg@juitsolan.in
Dr. Harsh Sohal,
8262054886, harsh.sohal@juitsolan.in

Connect with us on:
Facebook @ ECE.JUIT, Instagram @ juit_ece
LinkedIn @ Electronics & Communication Engineering, JUIT

About Jaypee University of Information Technology
JUIT was conceived by a joint vision of the Govt. of Himachal Pradesh and the Founder Chairman of Jaypee Group Shri Jai Prakash Gaur Ji in 2000. Being the first state private university we have the honor to have Governor of H.P. being the Chancellor. The JUIT is also a member of the Association of Indian Universities (AIU). The academic activities of JUIT commenced in July 2002 and currently offer undergraduate B.Tech. and M.Tech. degree programs in Bioinformatics, Biotechnology, Civil Engineering, Computer Science & Engineering, Electronics & Communication Engineering, Electronics & Computer Engineering, Civil Engineering with specialization in Computer Science and Information Technology. The University is also offering B.Sc., M.Sc.BBA and Ph.D. degree in different departments. The University campus is spread over 25 acres of lush green picturesque slopes of Wahnaghat hills in the Solan District of Himachal Pradesh. The smart campus is pollution free and enjoys lovely weather throughout the year.

About Department of Technical Education, Vocational and Industrial Training
The Directorate of Technical Education, Vocational and Industrial Training, Himachal Pradesh at Sundernagar is having the Administrative Control of its functional units in the State. The Department is responsible for providing Technical Education, Vocational & Industrial Training in the State at various levels i.e. ITIs, diploma courses for middle level technicians, undergraduate/ postgraduate in Engineering and Technology/Pharmacy. The Directorate has two Wings. The Technical Education Wing the Department has been entrusted with the responsibility of managing Degree and Diploma level Technical Institutions in the State of Himachal Pradesh. The Industrial Training Wing of the Department has been entrusted with the responsibility of imparting training in Engineering and non-engineering trades to cater to the needs of the industry in respect of skilled workers. Similar to the National Council for Vocational Training at the Central level, the State Council for Vocational Training at the State level is responsible for coordinating the integrated development of Industrial Training. The main motto of the technical institution is to provide superior quality trained manpower, having social commitment along with career advancement to meet the challenges and opportunities in thrown up by the fast evolving society in the 21st Century.

Objective of the Workshop
Very Large Scale Integration (VLSI) design is an important field that deals with the design and fabrication of integrated circuits. The proposed workshop provides **B.Tech/ B.Sc./ diploma / M.Tech.** students with necessary skills and knowledge to work in the field of VLSI design. The main objective of this workshop is to deliver the design aspects and provide hands-on experience with VLSI design tools like Cadence and Vivado (Xilinx) etc. in the Digital and Analog design domain where participants will get an extensive knowledge of the ideas and concepts of VLSI designs along with knowledge of FPGA.

Workshop will be conducted in Offline mode that comprises expert talks followed by Hands-on sessions. For registering the workshop, participants need to pay Rs. 500/- (Five hundred rupees only) which includes fooding and lodging charges for H.P. Certificates will be given to the attendees.
For Registration, visit: <http://tinyurl.com/juitecevlsi>

The resource persons invited for the workshop are experts in their domains and from the renowned Govt. Organizations/ Industry in the field of VLSI/Semiconductor are listed below:

1. Dr. H. S. Jattana, Former group head at SCL Mohali and ISRO
2. Dr. Satish Chandra Tiwari, DFT Manager (Principal Design Engineer), NXP Semiconductors
3. Dr. Balwinder Singh, Joint Director & Head, ACS Division, CDAC Mohali
4. Dr. Balwinder Raj, Associate Professor, NIT Jalandhar
5. Mr. Mayank Singh, Verification Engineer, NXP Semiconductor
6. Mr. Ankur Sangal, Technical Lead, HCL Technologies
7. Mr. Anish.K.Sharma, Sr. FAE, Entuple Technologies Pvt. Ltd.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



Jaypee University of Information Technology
Department of Electronics & Communication Engineering
In collaboration with
Department of Technical Education , Vocational & Industrial Training,
Government of Himachal Pradesh

**One-week Hands-on Workshop on “VLSI Design”
(04th - 09th March, 2024)**



Dr. Harpreet S. Jatana
Former group head
SCL Mohali and ISRO



Dr. Balwinder Singh
Joint Director&Head,
ACS Division, CDAC
Mohali



Dr. Balwinder Raj
Associate Professor
NIT Jalandhar



Dr. Satish C. Tiwari
DFT Manager,
NXP Semiconductors,
INDIA



Mr. Mayank Singh,
Verification Engineer,
NXP Semiconductor



Mr. Ankur Sangal
Technical Lead
HCL Technologies



Mr. Anish.K.Sharma,
Sr. FAE, Entuple
Technologies

The workshop was inaugurated by Dr. Satish Chandra Tiwari, DFT Manager (Principal Design Engineer) at NXP Semiconductors, INDIA. The inaugural ceremony, graced by esteemed guests Mr. Mayank Singh, Verification Engineer at NXP Semiconductor, and Mr. Ankur Sangal, Technical Lead at HCL Technologies, marked the beginning of an insightful event. The inaugural session witnessed the presence of key figures, including Prof. Rajendra Kumar Sharma, Vice-Chancellor of JUIT, Prof. Ashok Kumar Gupta, Dean (Academics & Research), Maj Rakesh Bassi, Dean of Student Welfare, Prof. P.B. Barman, Head of the Department (PMS), Prof. Rajiv Kumar, Head of the Department (ECE), and Prof. Dr. Shruti Jain, Associate Dean (Innovation). Dr. Harsh Sohal and Dr. Pardeep Garg steered the coordination of the workshop, ensuring its success and providing a platform for participants to delve into the intricacies of VLSI Design.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

Itinerary

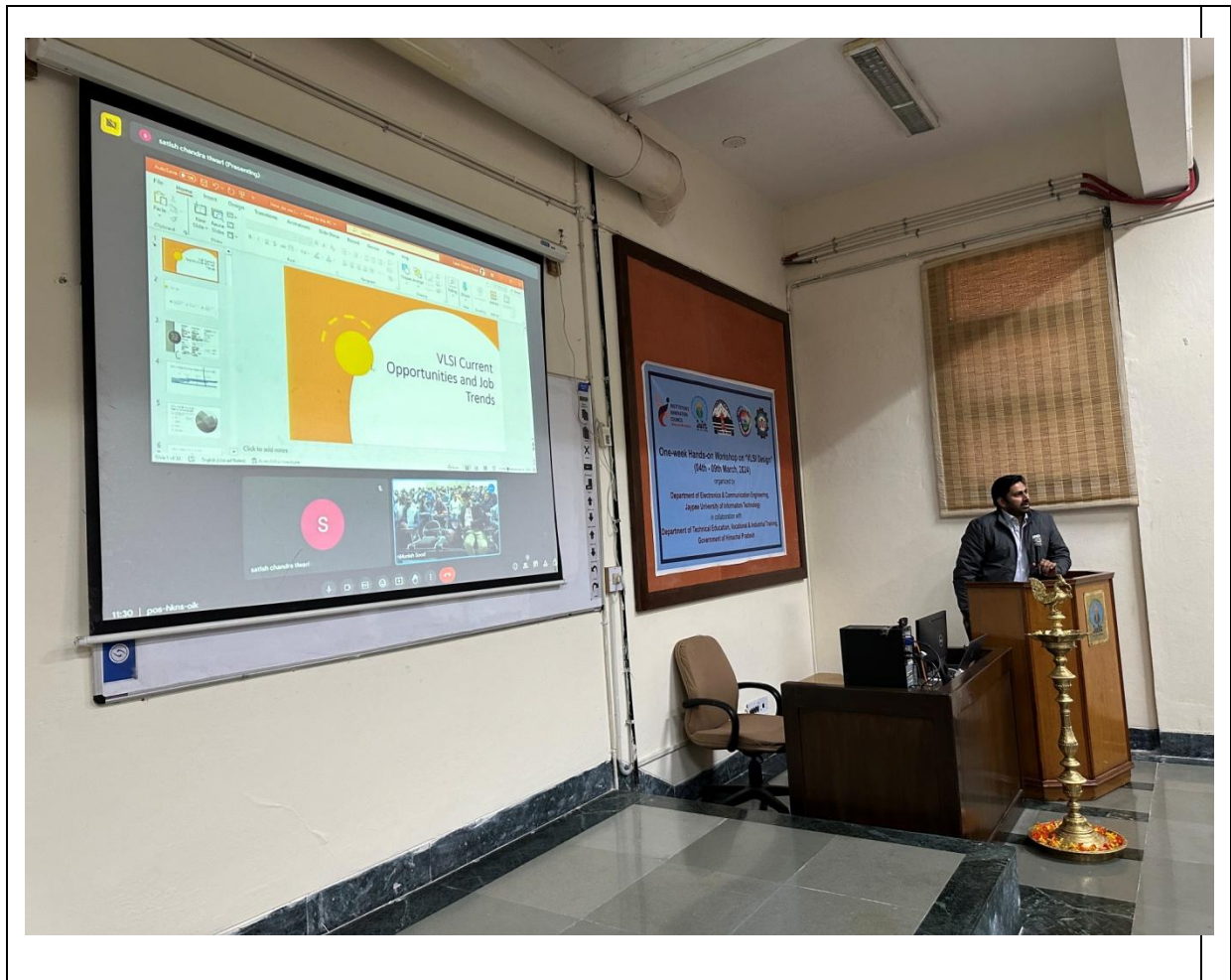
Registration Time: 9:00 AM (Academic Block, Vivekanand Bhawan)

Date	Time	Events (ALL IN CL1, 2nd floor, Vivekanand Bhawan)
04-03-2024	10:00AM	Inaugural function
	10: 30 AM	Expert Lecture by Dr. Satish Chandra Tiwari , DFT Manager (Principal Design engineer), NXP Semiconductors, INDIA. VLSI Current opportunities and Job Trends
	2:30 PM	Hand's on session by Mr. Mayank Singh , Verification Engineer, NXP Semiconductor (Consultant) RTL VERIFICATION
05-03-2024	10:00AM	Expert Lecture by Xilinx Vivado Tool Flow with FPGA based coding techniques by Mr. Ankur Sangal , Technical Lead, HCL Technologies Hand's on session by Mr. Mayank Singh , Verification Engineer, NXP Semiconductor.
	2:30 PM	Hand's on session IP Integrator using Xilinx Vivado Tool by Mr. Ankur Sangal , Technical Lead, HCL Technologies
06-03-2024	10:00AM	Expert Lecture by Dr. Balwinder Singh , Joint Director & Head, ACS Division, CDAC Mohali SoC Testing and hardware security concerns
	2:30 PM	Hand's on session by Dr. Balwinder Singh
07-03-2024	10:00AM	Expert Lecture by Mr. Anish.K.Sharma , Sr. FAE, Entuple Technologies Pvt. Ltd
	2:30 PM	Hand's on session by, Mr. Anish.K.Sharma on Cadence
08-03-2024	10:00AM	Expert Lecture by Dr. Balwinder Raj , Associate Professor, NIT Jalandhar Multi-Gate Semiconductor Devices for VLSI Design
	2:30 PM	Hand's on session by, Mr. Anish.K.Sharma on Cadence
09-03-2024	9:30 AM	Expert Lecture by Dr. Harpreet Singh Jatana , Former group head at SCL Mohali and ISRO. Challenges in CMOS design in low geometry technology node
	11:30 AM	Valedictory

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

After the inauguration at around 11:00 AM, Dr. Satish Chandra Tiwari delivered his talk on the topic 'VLSI Current opportunities and Job Trends'.



JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

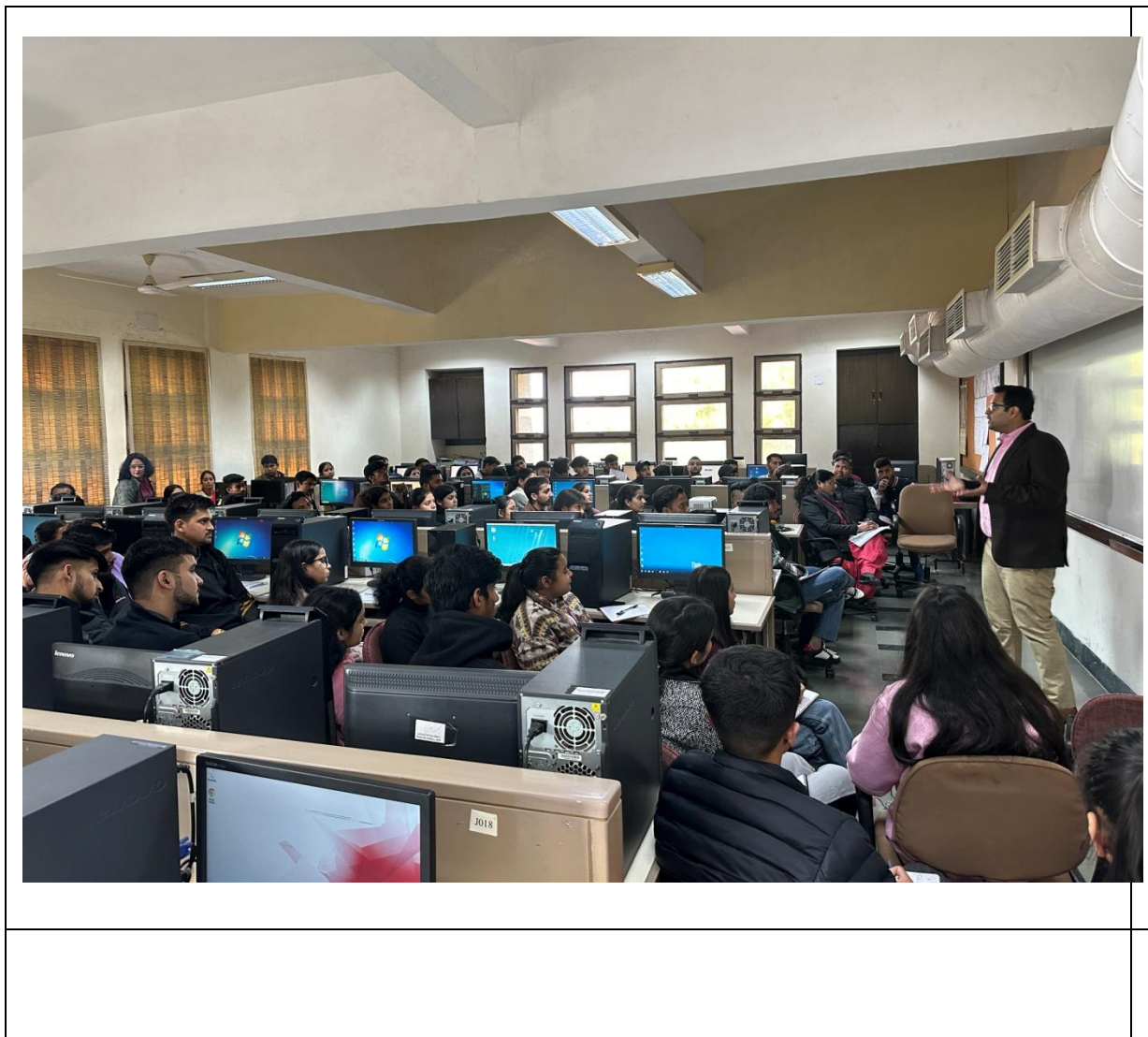
(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the afternoon on 04-03-2024, Mr. Mayank Singh started his talk with Verilog HDL based implementation of Digital Logic Blocks and specifically covered the topic ‘RTL VERIFICATION’.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the morning session on 05-03-2024, Mr. Ankur Sangal delivered his expert lecture on the topic, 'Xilinx Vivado Tool Flow with FPGA based coding techniques'. The participants were successfully able to perform the hands on experiments and hence learnt to use the Xilinx Vivado Tool flow to design basic digital logic and also to burn the same on to ZedBoard (Zynq-7000 ARM/FPGA SoC Development Board).

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the afternoon on 05-03-2024, Mr. Mayank Singh completed his talk on the topic ‘RTL VERIFICATION’. He discussed with the participants the basic concepts which are very important for the new entrants to grasp and practice. He also shared some questions which he generally asks the aspirants while he interviews them for his verification team.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the morning session on 06-03-2024, Dr. Balwinder Singh introduced the participants to system of chip while focussing on, 'SoC Testing and hardware security concerns'. He also stressed the hardware security concerns as one of the driving forces behind the Government of India Semiconductor initiative.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

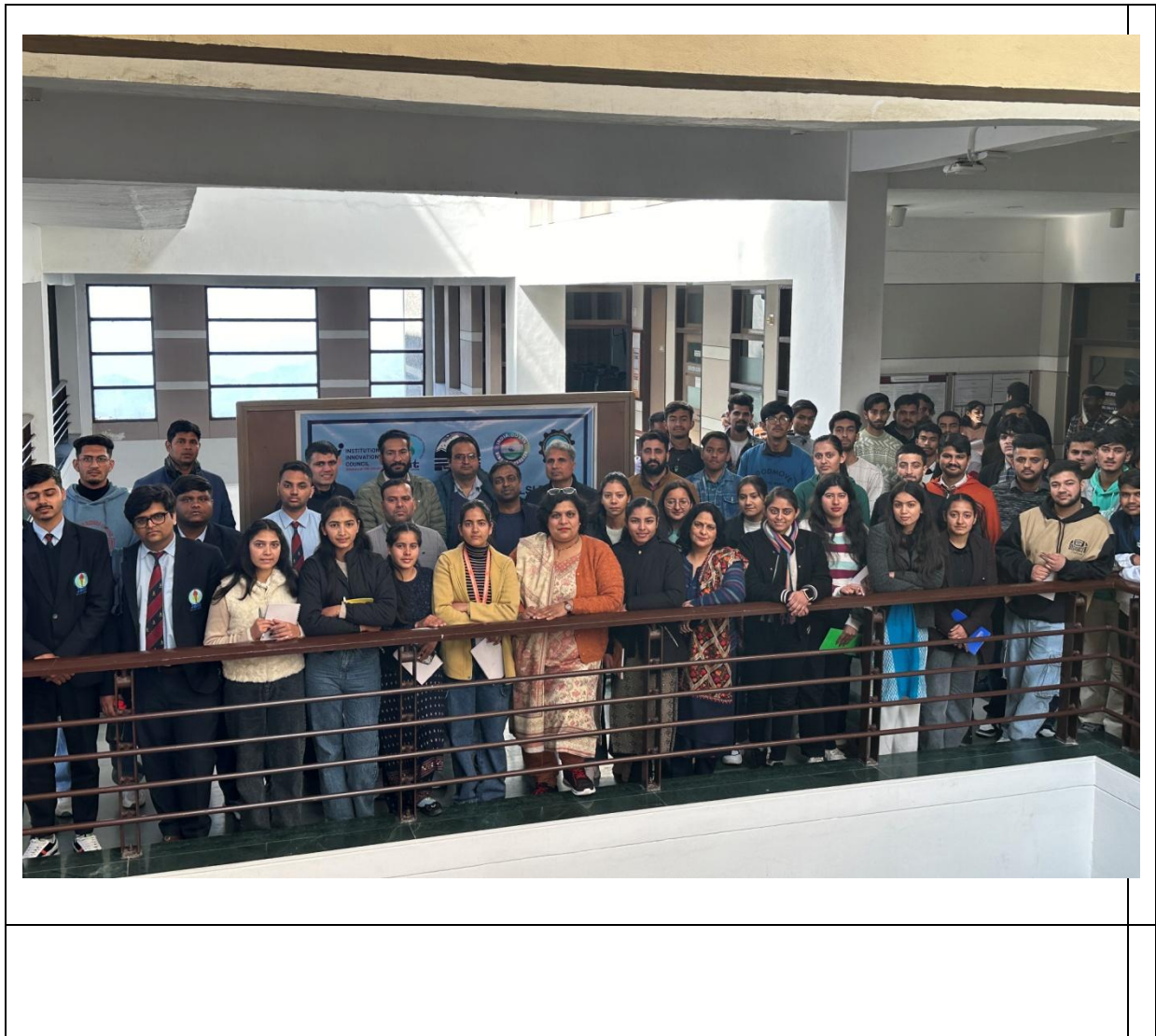
(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the afternoon session on 06-03-2024, Dr. Balwinder Singh took the hands on session and covered the concept of VLSI design using Cadence Virtuoso tool.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



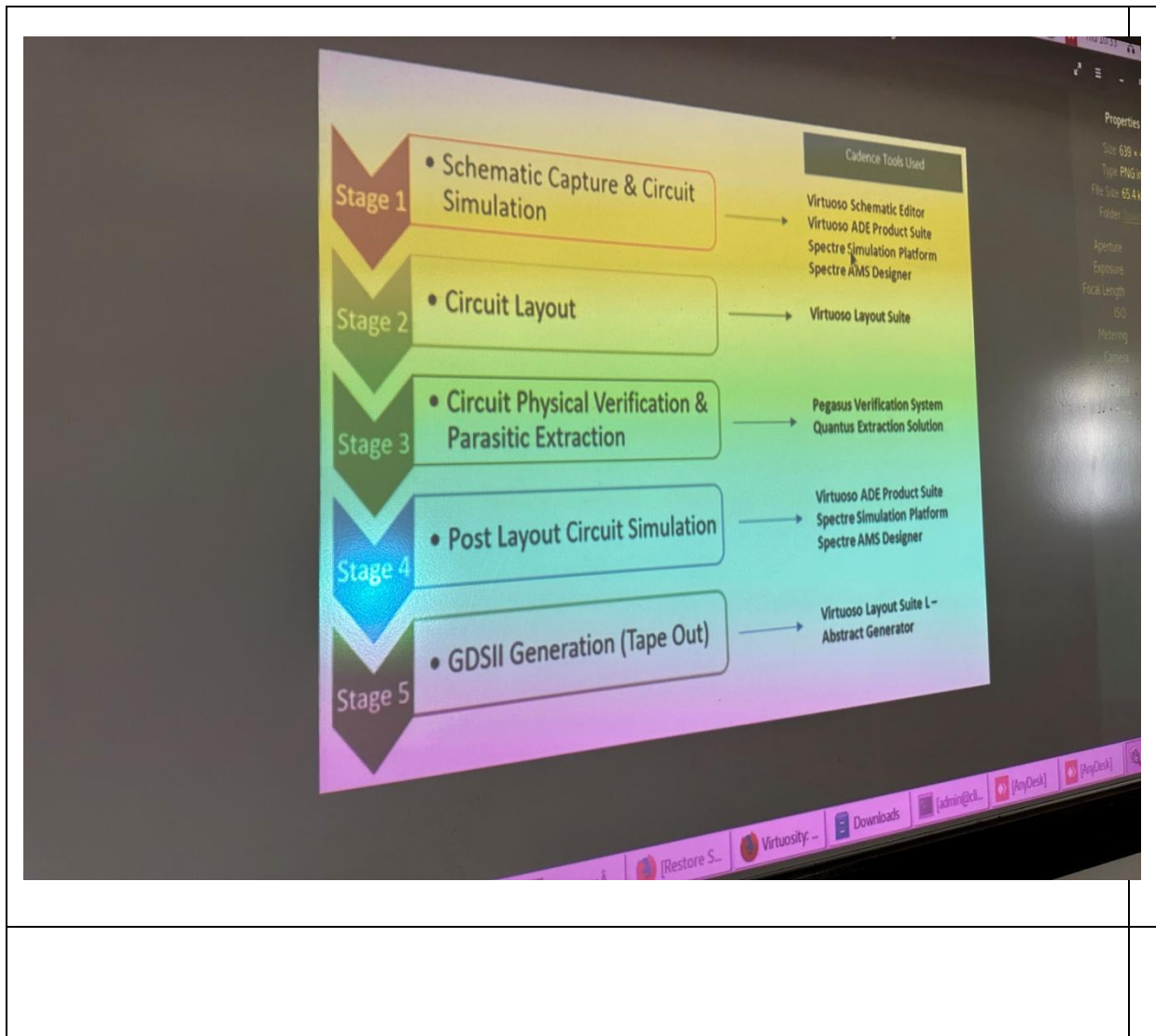
In the morning session on 07-03-2024, Mr. Anish Kumar Sharma delivered his expert lecture on the topic, 'EDA Tools'.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the afternoon session on 07-03-2024, Mr. Anish Kumar Sharma took the hands on session and covered the concept of VLSI design using Cadence Virtuoso tool. The focus of the session was to familiarise the participants in the Digital Design flow of the Cadence Virtuoso EDA tool.



In the morning session on 08-03-2024, Dr. Balwinder Raj delivered his expert lecture on the topic, 'Multi-Gate Semiconductor Devices for VLSI Design'. Dr. Balwinder Raj presented to the audience his research work in the area of Semiconductor Devices. He introduced the participants to the future of semiconductor industry beyond traditional 'Si' as a material approach.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

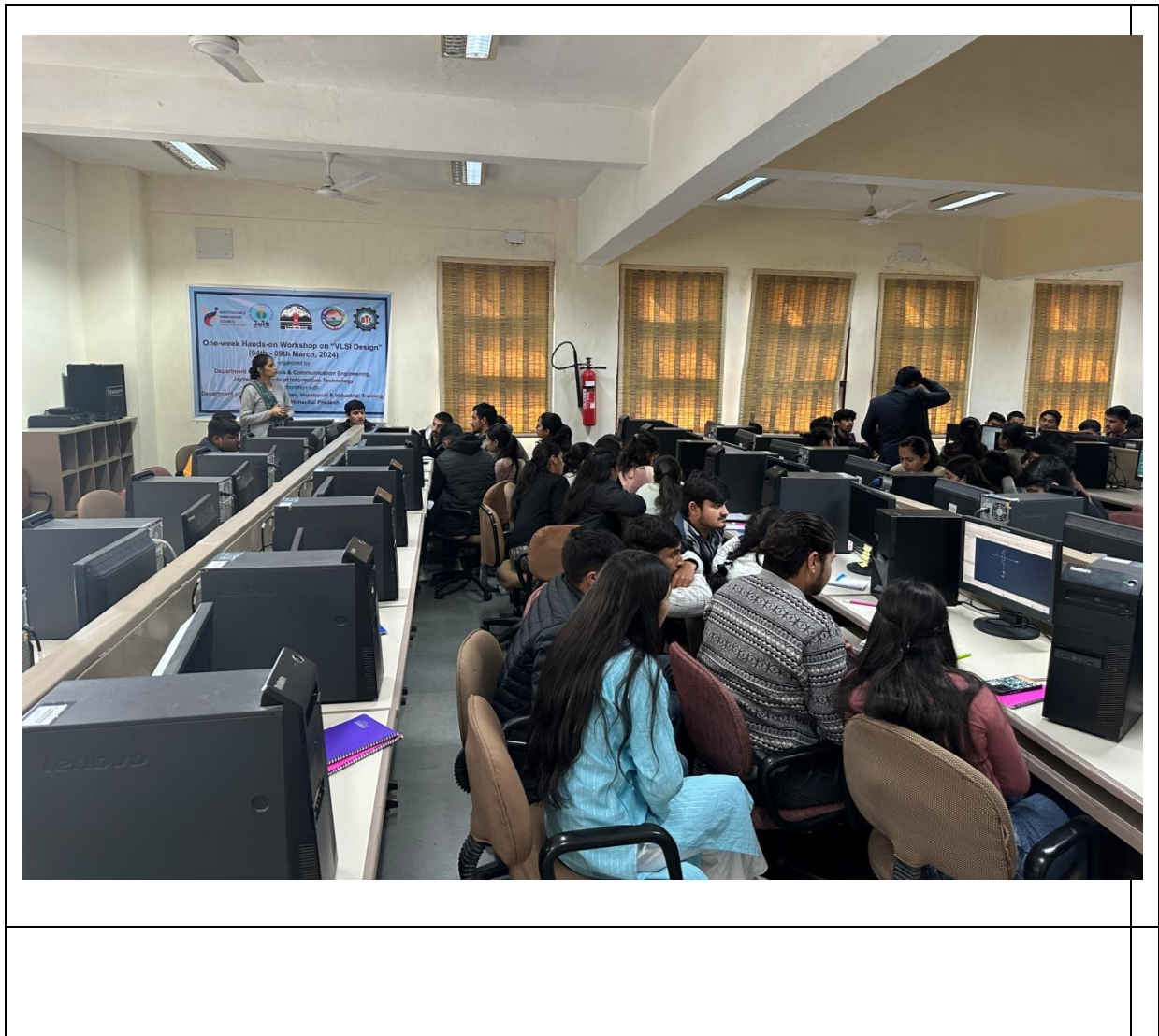
(Established by H.P. State Legislature vide Act No. 14 of 2002)



In the afternoon session on 08-03-2024, Mr. Anish Kumar Sharma took the hands on session and covered the concept of VLSI design using Cadence Virtuoso tool.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



The last session of the workshop commenced on the morning of 09-03-2024 with the expert lecture of Dr. Harpreet Singh Jattana titled, "Challenges in CMOS design in low geometry technology node". After the talk was over he interacted with the students while discussing the GoI policy initiatives, various companies working for the semiconductor industry. Also, he showed the Silicon Wafer to the participants.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



At 11:30 AM on 09-03-2024, the valedictory session was conducted; the certificates were distributed to all the participants and the Workshop organizers.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)



This collaborative endeavour between academia and industry experts promises to equip the participants with invaluable insights and hands-on experiences in the dynamic domain of VLSI Design. As JUIT continues to foster academic excellence, such workshops contribute significantly to shaping the future of aspiring engineers and innovators. The participants are set to gain practical knowledge, opening doors to new possibilities and reinforcing JUIT's commitment to nurturing talent in cutting-edge technological domains. The workshop was structured to be highly interactive, incorporating hands-on exercises utilizing industry-standard EDA tools. Participants engaged in designing, simulating, and verifying digital circuits under the guidance of experienced professionals. The comprehensive curriculum covered fundamental VLSI design principles, ensuring participants acquired practical skills essential for further studies or careers in the field. The week-long event facilitated a unique opportunity for attendees to directly interact with industry experts, fostering insightful discussions and enabling valuable networking among participants. As the workshop concluded, participants left with a solid foundation in VLSI design and the confidence to pursue advanced studies or embark on careers within the dynamic, lucrative realm of VLSI/Semiconductors.

The success of the "VLSI Design" workshop underscored JUIT Solan's commitment to providing students with hands-on learning experiences and industry-relevant knowledge, thereby contributing to the advancement of technology in the region. Participants gained a solid understanding of VLSI design principles and methodologies. They will surely aspire to enhance their problem-solving and critical thinking skills in the field of VLSI design.

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

Participants:

S. No.	Name	Currently enrolled in:	University/ College/ School Name	City/State	Gender
1	Avantika Sharma	B.Tech.	Rajiv Gandhi Government Engineering College	Himachal Pradesh	Female
2	Sonika devi	B.Tech.	Rajiv Gandhi government engineering college, massal	Nagrota bagwan	Female
3	Sumit Attar	B.Tech.	Rajiv Gandhi government engineering college at nagrota bagwan	Kangra/Himachal Pradesh	Male
4	ANUJ SHARMA	Diploma	Govt. Millennium Polytechnic Chamba	CHAMBA (H.P.)	Male
5	Rishu Sharma	Diploma	Govt. Millennium Polytechnic Chamba	Himachal Pradesh	Male
6	Karan singh	Diploma	Govt. Millennium polytechnic Chamba	Chamba	Male
7	Abhishek Kumar	Diploma	Govt. Millennium polytechnic Chamba	Himachal Pradesh	Male
8	Ajay Kumar	Diploma	Govt. Millennium polytechnic Chamba	Himachal Pradesh	Male
9	Abhishek Kumar	Diploma	Government Millennium Polytechnic Chamba	Chamba (Himachal Pradesh)	Male
10	Aman Bharwal	Diploma	Dr. B. R. Ambedkar Govt. Polytechnic Ambota	Gagret / Himachal Pradesh	Male
11	Sahil Naryal	Diploma	Dr Br Ambedkar govt polytechnic Ambota	Gagret/ Himachal pardesh	Male
12	Sunil kumar	Diploma	Dr. Br. Ambedkar govt. Polytechnic Ambota	Una/H.p.	Male
13	Rihal Rai	Diploma	Dr. B. R. Ambedkar Govt. Polytechnic Ambota	Gagret/ Himachal Pradesh	Male
14	Kritika	Diploma	Dr. B.R Ambedkar Govt. Polytechnic Ambota	Gagret/Himachal Pradesh	Female
15	Sunidhi Rana	Diploma	Dr. B.R Ambedkar Govt. Polytechnic Ambota	Gagret/ Himachal Pradesh	Female
16	Lovely vijay banta	Diploma	Government Polytechnic Rohru	Shimla	Male
17	Amish kumar	Diploma	Government Polytechnic Rohru	Shimla	Male

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

18	Rajat	Diploma	Government Polytechnic Rohru	Shimla	Male
19	ANSHUL KESTA	M.Tech.	Govt. Polytechnic Rohru	Shimla	Male
20	Rishu	Diploma	Government Polytechnic Rohru	Shimla	Male
21	Sparsh verma	Diploma	Government polytechnic Rohru	Shimla	Male
22	Aayush	Diploma	Government Polytechnic Rohru	Shimla	Male
23	Dhananjay Sharma	Diploma	Government Polytechnic Rohru	Rohru	Male
24	Ankit Kumar	Diploma	Government Polytechnic Rohru	Shimla	Male
25	Parikshit Sharma	Diploma	Govt. Polytechnic Hamirpur	Hamirpur	Male
26	Anish Malhotra	Diploma	Govt. Polytechnic hamirpur	Hamirpur	Male
27	Nikhil Moudgil	Diploma	Govt Polytechnic Hamirpur	Hamirpur	Male
28	Mayank Chauhan	Diploma	Govt. Polytechnic Paonta Sahib	Himachal Pradesh	Male
29	Harpreet Singh	Diploma	Govt. Polytechnic Paonta Sahib	Himachal Pradesh	Male
30	Tarun Kashyap	Diploma	Govt. Polytechnic Paonta Sahib	Himachal Pradesh	Male
31	Anamika	Diploma	Govt.polytechnic Sundernagar	Sundernagar	Female
32	Deepa Devi	Diploma	Government Polytechnic Sundernagar	Sundernagar	Female
33	Dhruv Sharma	Diploma	Govt polytech Sundernagar	Sundernagar	Male
34	Manish Kumar	B.Tech.	Jawaharlal Nehru Govt. Engineering Collage Sundernagar	Himachal Pradesh	Male
35	Tanishq Sood	B.Tech.	Jawaharlal Nehru Govt. Engineering Collage Sundernagar	Himachal Pradesh	Male
36	Sarthak Patial	B.Tech.	Jawaharlal Nehru Government Engineering College	Sundernagar	Male

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

37	Aryan Sharma	B.Tech.	Jawaharlal Nehru Government Engineering College	Sundernagar	Male
38	Diya Sharma	B.Tech.	Jawaharlal Nehru Government Engineering College	SunderNagar	Female
39	Shruti Sharma	B.Tech.	Jawaharlal Nehru government engineering College, Sundernagar	Sundernagar	Female
40	SURYA SHARMA	Diploma	Government Polytechnic Kangra	Kangra / Himachal Pradesh	Male
41	AVDESH KUMAR	Diploma	Government Polytechnic Kangra	Kangra, Himachal Pradesh	Male
42	SUSHEN DHIMAN	Diploma	Government Polytechnic Kangra	Kangra, Himachal Pradesh	Male
43	Kamal Kumar	Diploma	Government Polytechnic College Kangra	Kangra	Male
44	Nikhil	Diploma	Government polytechnic Kangra	Kangra	Male
45	Rishav	Diploma	Government Polytechnic Kangra	Kangra	Male
46	Neha Sharma	Diploma	G.P.W Kandaghat	solan	Female
47	Anshita	Diploma	Government polytechnic for women kandaghat	Kandaghat / solan	Female
48	Sonia	Diploma	G.P.W Kandaghat	Solan	Female
49	Sakshi	Diploma	GPW Kandaghat	Kandaghat	Female
50	Niharika	Diploma	GPW kandaghat	Solan	Female
51	Pooja Devi	Diploma	Govt. Polytechnic for Women Rehan	Himachal Pradesh	Female
52	Komal	Diploma	Govt. Polytechnic for Women Rehan	Himachal Pradesh	Female
53	Nidhi Sharma	Diploma	Govt. Polytechnic for Women Rehan	Himachal Pradesh	Female
54	Neha	Diploma	Government polytechnic for women Kandaghat	Kandaghat	Female
55	Ipshita Puri	B.Tech.	Government Hydro Engineering College Bandladhar , Bilaspur	HP	Female

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY

(Established by H.P. State Legislature vide Act No. 14 of 2002)

56	Bhanupriya	B.Tech.	Government Hydro Engineering College Bandla Bilaspur	H.P	Female
57	Sakshi Sharma	B.Tech.	Govt.Hydro Engineering College Bandla , Bilaspur (H.P)	H.P	Female
58	Ankita Saini	B.Tech.	ABVGIET Pragtinagar	Himachal Pradesh	Female
59	Nitish kunar	B.Tech.	ABVGIET Pragtinagar	Himachal pradesh	Male
60	Chhering Dolma	B.Tech.	ABVGIET Pragtinagar	Himachal Pradesh	Female
61	Ashish Kumar	Diploma	ABVGIET Pragtinagar	Shimla	Male
62	Pankaj Kumar	Diploma	ABVGIET Pragtinagar	Shimla	Male
63	Alisha	B.Tech.	AVBGIET pragati nagar	Himachal Pradesh	Female
64	Ankita Thakur	Diploma	ABVGIET Pragtinagar	Shimla	Female
65	Sarika Sharma	B.Tech.	ABVGIET Pragtinagar	Himachal Pradesh (Hamirpur)	Female
66	Shivani Gaura	B.Tech.	ABVGIET Pragtinagar	Himachal Pradesh	Female
67	Tanishk Thakur	M.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Male
68	Rishika Goel	M.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Female
69	Naresh Rana	M.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Male
70	Aaryan Sharma	B.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Male
71	Prakhar Kulshrestha	B.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Male
72	Sandeep Thakur	Faculty	ABVGIET Pragtinagar	Himachal Pradesh	Male
73	Navya	B.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Female
74	Manas Jain	B.Tech.	Jaypee University of Information Technology, Solan	Himachal Pradesh	Male

Newspaper clippings:



Guests from various universities attending a workshop organised at JUIT on Monday.

Workshop on "VLSI Design" inaugurated at JUIT

Excelsior Correspondent at JUIT in collaboration with the Department of Technical Education, Vocational and Industrial Training, Government of Himachal Pradesh. There were more than 80 participants from various districts of Himachal Pradesh.

JAMMU, Mar 4: A week long Workshop on "VLSI Design" was inaugurated at Jaypee University of Information Technology, (JUIT) Waknaghat, Solan here today. The workshop was inaugurated by Dr. Satish Chandra Tiwari, DFT Manager (Principal Design Engineer), NXP Semiconductors, INDIA, who also was the Chief Guest. Mayank Singh, Verification Engineer, NXP Semiconductor and Ankur Sangal, Technical Lead, HCL Technologies were the Guest of Honor.

The workshop was organized

Prof. Rajendra Kumar Sharma, VC, Prof. Ashok Kumar Gupta, Dean (A&R), Maj Rakesh Bassi, Dean Student Welfare, Prof. P.B. Barman, HoD PMS, Prof. Rajiv Kumar, HoD ECE and Prof. Dr. Shruti Jain, Associate Dean (I) graced the inaugural of the workshop.

Dr. Harsh Sohal and Dr. Pardeep Garg are the coordinators of the event.

जेपी यूनिवर्सिटी में वीएलएसआई डिजाइन पर व्यावहारिक कार्यशाला का आयोजन

हिमाचल दस्तक ब्यूरो | सोलन

वीएलएसआई डिजाइन पर एक सप्ताह की व्यावहारिक कार्यशाला का उद्घाटन मुख्य अतिथि के रूप में डॉ. सतीश चंद्र तिवारी, डीएफटी मैनेजर (प्रिंसिपल डिजाइन इंजीनियर), एनएक्सपी सेमीकंडक्टर, इंडिया ने किया। मरक सिंह, सत्यापन अभियंता, एनएक्सपी सेमीकंडक्टर और अंकुर संगल, तकनीकी प्रमुख, एचसीएल टेक्नोलॉजी सम्मानित अतिथि थे। प्रो. राजेंद्र कुमार शर्मा वीसी, प्रो. अशोक कुमार गुप्ता डीन (ए&आर), मजर राकेश बस्सी, डीन छात्र

कार्यक्रम में प्रदेश के विभिन्न जिलों से 80 से अधिक प्रतिभागी शामिल



कल्याण, प्रो. पीबो बर्मन, एचओडी पीएमएस, प्रोफेसर राजीव कुमार, इसीई विभागाध्यक्ष और प्रो. डॉ. श्रुति जैन, एसोसिएट डीन (आई) ने कार्यशाला के उद्घाटन की शोभा बढ़ाई। डॉ. हर्ष सोहल और डॉ. प्रदीप गर्ग कार्यक्रम के समन्वयक रहे। कार्यशाला का आयोजन इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग विभाग, जेपी सूचना प्रौद्योगिकी विश्वविद्यालय, (जेयूआईटी) वाकनाघाट, सोलन द्वारा तकनीकी शिक्षा, व्यावसायिक और औद्योगिक प्रशिक्षण विभाग, हिमाचल प्रदेश सरकार के सहयोग से किया गया। कार्यक्रम 4 से 9 मार्च तक जेयूआईटी वाकनाघाट परिसर में निर्धारित है। इसमें हिमाचल प्रदेश के विभिन्न जिलों से 80 से अधिक प्रतिभागी शामिल हैं।

10:42

< Pun-01_merged (4)-73

करन वाला कालर न्यूनतम वतन 5,500।सगापुर डालर स बढाकर 6,200 सिगापुर डालर कर दिया गया है। इस क्षेत्र में अधिक वतन के रुझानों को देखते हुए ऐसा किया गया है। नया वतनमान इंधी धारकों पर तब लागू होगा, जब वे एक साल बाद पास का नवीनीकरण कराएंगे।

म यह कहा गया है। दश क माड और मनोरंजन (एम एंड ई) क्षेत्र 2023 में 8.1 प्रतिशत की वृद्धि और यह 2.32 लाख करोड़ रु

बीते साल बेरोजगारी दर घटकर 3.1 प्रतिशत पर आ

सर्वेरा न्यूज/एजेंसी
नई दिल्ली, 5 मार्च : सांख्यिकी मंत्रालय के राष्ट्रीय नमूना सर्वेक्षण संगठन ने कहा है कि 15 साल या उससे अधिक उम्र के लोगों की बेरोजगारी दर वर्ष 2023 में घटकर 3.1 प्रतिशत रह गई, जो तीन साल का सबसे निचला स्तर है। राष्ट्रीय

2022 में यह दर 3.6 प्रतिशत और 2021 में 4.2 प्रतिशत रही थी

नमूना सर्वेक्षण संगठन (एनएसएसओ) की तरफ से मंगलवार को जारी आवधिक श्रमबल सर्वेक्षण रिपोर्ट के मुताबिक, कैलेंडर वर्ष 2023 में देश की बेरोजगारी दर

3.1 प्रतिशत रही जबकि 2022 में यह 3.6 प्रतिशत और 2021 में 4.2 प्रतिशत रही थी। बेरोजगारी दर के श्रमबल (15 साल से अधिक उम्र वर्ग) में बेरोजगार लोगों के प्रतिशत के रूप में परिभाषित किया जाता है आंकड़ों के मुताबिक, देश में कोविड महामारी का मार्च, 2020 में प्रसा

‘वीएलएसआई डिजाइन’ पर एक सप्ताह की व्यावहारिक कार्यशाला का उद्घाटन



सर्वेरा न्यूज
नई दिल्ली, 5 मार्च : वीएलएसआई डिजाइन पर एक सप्ताह की व्यावहारिक कार्यशाला का उद्घाटन मुख्य अतिथि के रूप में डा. सतीश चंद्र तिवारी, डीएफटी मैनेजर (प्रिंसिपल डिजाइन इंजीनियर), एनएक्सपी सेमीकंडक्टर, इंडिया ने किया। कार्यशाला का आयोजन इलेक्ट्रॉनिक्स और संचार इंजीनियरिंग विभाग, जेपी सूचना प्रौद्योगिकी विश्वविद्यालय, (जेयूआईटी) वाकनाघाट, सोलन द्वारा तकनीकी शिक्षा, व्यावसायिक और औद्योगिक

प्रशिक्षण विभाग, हिमाचल प्रदेश सरकार के सहयोग से किया गया था। मयंक सिंह, सत्यापन अभियंता, एनएक्सपी सेमीकंडक्टर और श्री अंकुर संगल, तकनीकी प्रमुख, एचसीएल टेक्नोलॉजीज सम्मानित अतिथि थे। प्रो. राजेंद्र कुमार शर्मा; वीसी, प्रो. अशोक कुमार गुप्ता; डीन (ए एंड आर), मेजर राकेश वर्मा, डीन छात्र कल्याण, प्रो. पी.बी.वर्मा; एचओडी पीएमएस, प्रोफेसर राजीव कुमार; ईसीई विभागाध्यक्ष और प्रो. डॉ. श्रुति जैन; एसोसिएट डीन (आई) ने कार्यशाला के उद्घाटन की

शोभा बढ़ाई। डा हर्ष सोहल और डा प्रदीप गर्ग कार्यक्रम के समन्वयक हैं।



क्र. सं.	विभाग का नाम
1.	निदेशक, फूड सिविल सप्लायर्स एवं उपभोक्ता मामले, पंचाय, चंडीगढ़
2.	निदेशक, फूड सिविल सप्लायर्स एवं उपभोक्ता मामले, पंचाय, चंडीगढ़

अन्य जानकारी और शुद्धिपत्र तथा एड्रेस

Online prints:

1. <https://himachaltonite.com/himachal/juit-solan-hosts-successful-vlsi-design-workshop/>
2. <https://crazynewsindia.com/breaking-news-flash-news/vlsi-design-workshop-held-at-juit/>
3. <https://shikharnewsindia.com/archives/3319>
4. <https://himachaltonite.com/education/one-week-hands-on-workshop-on-vlsi-design-inaugurated-at-juit-waknaghat-campus/>
5. <https://crazynewsindia.com/breaking-news-flash-news/report-on-one-week-hands-on-workshop-on-vlsi-design-held/>