Virtual Lab, IIT-Kharagpur: Computer Organization and Architecture

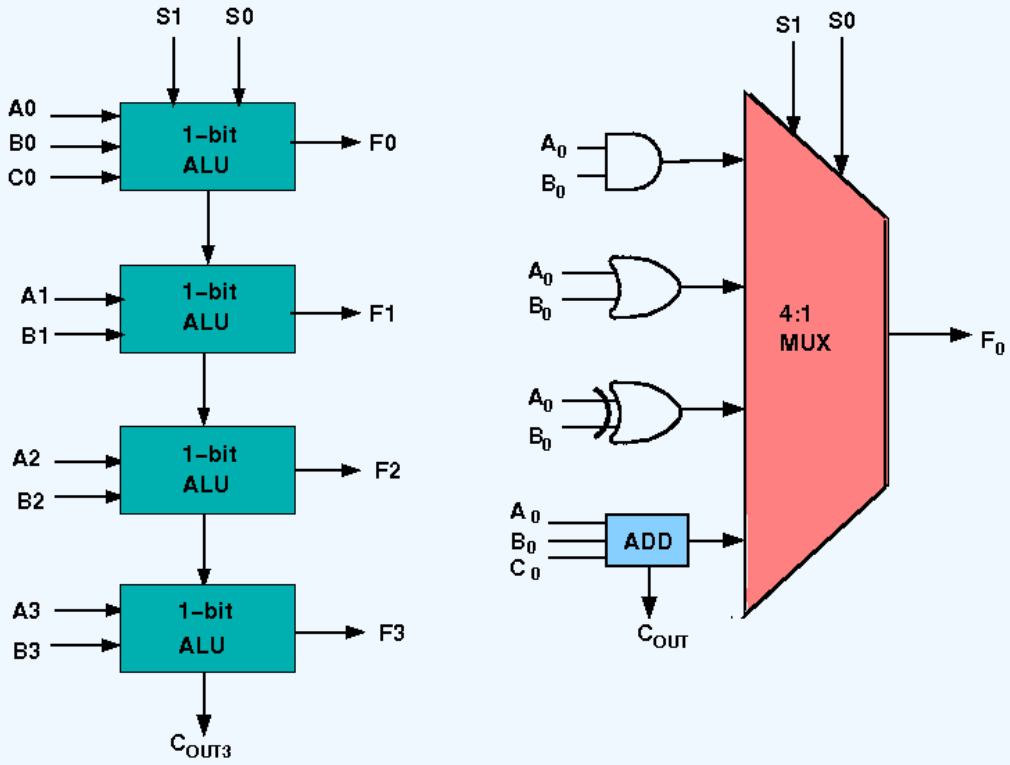
JUIT Regular Lab: Computer Organization and Architecture (10B11CI613)

1. Design of ALU
2. Objective of memory design (single bit RAM cell)

Theory

Exp-1. Design of ALU:

ALU or Arithmetic Logical Unit is a digital circuit to do arithmetic operations like addition, subtraction, division, multiplication and logical operations like and, or, xor, nand, nor etc. A simple block diagram of a 4 bit ALU for operations and, or, xor and Add is shown here:



The 4-bit ALU block is combined using 4 1-bit ALU block

Design Issues :

The circuit functionality of a 1 bit ALU is shown here, depending upon the control signal S_1 and S_0 the circuit operates as follows:

for Control signal **$S_1 = 0$** , $S_0 = 0$, the output is **A And B**,

for Control signal **$S_1 = 0$** , $S_0 = 1$, the output is **A Or B**,

for Control signal $S_1 = 1$, $S_0 = 0$, the output is **A Xor B**,

for Control signal $S_1 = 1$, $S_0 = 1$, the output is **A Add B**.

The truth table for 16-bit ALU with capabilities similar to 74181 is shown here:

Required functionality of ALU (inputs and outputs are active high)

Mode Select Inputs				**F_n for active HIGH operands**	
				Logic	**Arithmetic (note 2)**
S3	S2	S1	S0	(M = H)	(M = L) **(C_n=L)**
L	L	L	L	A'	A
L	L	L	H	A'+B'	A+B
L	L	H	L	A'B	A+B'
L	L	H	H	Logic 0	minus 1
L	H	L	L	(AB)'	A plus AB'
L	H	L	H	B'	(A + B) plus AB'
L	H	H	L	A ⊕ B	A minus B minus 1
L	H	H	H	AB'	AB minus 1
H	L	L	L	A'+B	A plus AB
H	L	L	H	(A ⊕ B)'	A plus B
H	L	H	L	B	(A + B') plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logic 1	A plus A (Note 1)
H	H	L	H	A+B'	(A + B) plus A
H	H	H	L	A+B	(A + B') plus A
H	H	H	H	A	A minus 1

The L denotes the logic low and H denotes logic high.

Objective of 4 bit arithmetic logic unit(with AND, OR, XOR, ADD operation):

1. Understanding behaviour of arithmetic logic unit from working module and the module designed by the student as part of the experiment
2. Designing an arithmetic logic unit for given parameter

Examining behaviour of arithmetic logic unit for the working module and module designed by the student as part of the experiment (refer to the circuit diagram):

Loading data in the arithmetic logic unit (refer to procedure tab for further detail and experiment manual for pin numbers):

- load the two input numbers as:
  - A(A3 A2 A1 A0): A3=1, A2=1, A1=0, A0=0
  - B(B3 B2 B1 B0): B3=1, B2=0, B1=0, B0=1
  - carry in(C0)=0

examining the AND behaviour:

- load data in select input as:
  - S1=0, S0=0 `

- check output:
  - F3=1, F2=0, F1=0, F0=0
  - cout=0 `

examining the OR behaviour:

- load data in select input as:
  - S1=0, S0=1 `

- check output:
  - F3=1, F2=1, F1=0, F0=1
  - cout=0 `

examining the XOR behaviour:

- load data in select input as:
  - S1=1, S0=0 `

- check output:
  - F3=0, F2=1, F1=0, F0=1
  - cout=0 `

examining the ADD behaviour:

- load data in select input as:
  - S1=1, S0=1 `

- check output:
  - F3=0, F2=1, F1=0, F0=1
  - cout=1 `

- color configuration of wire for 5 valued logic supported by the simulator:

  - if value is UNKNOWN, wire color= maroon
  - if value is TRUE, wire color= blue
  - if value is FALSE, wire color= black
  - if value is HI IMPEDENCE, wire color= green
  - if value is INVALID, wire color= orange

likewise the 16 bit arithmetic logic unit can be designed and tested

- by cascading 4 bit ALUs only the carry will propagate to the next level for ADD operation

Test plan :

1. Set inputs 0101 and 0011 and check output for all possible select input combinations.
2. Set any two 16-bit number and check output for all possible select input combinations.

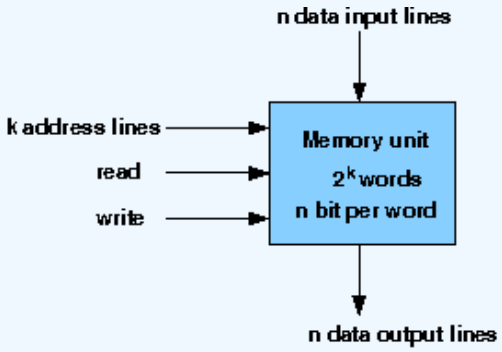
Use Display units for checking output. Try to use minimum number of components to build. The pin configuration of the canned components are shown when mouse hovered over a component.

Assignment Statements:

1. Design a 4 bit ALU comprising only the AND, OR, XOR and Add operations.
2. Design a 16-bit ALU with capabilities similar to 74181

Exp-2. Design of Memory :

A memory unit is a collection of storage cells together with associated circuits needed to transform insformation in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location is called random access memory(RAM). The block diagram of a memory unit-



Internal Construction: The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

RAM Design:

Design of a RAM Cell

Design of a 4X4 RAM

Design Issues :

A basic RAM cell has been provided here as a component which can be used to design larger memory units. An IC memory consisting of 4 words each having 3 bits has been aslo provided.

Objective of memory design (single bit RAM cell):

To design memory units and understand how it operates during read and write operation.

1. understanding behaviour of memory from working module and the module designed by the student as part of the experiment
2. designing an memory for given parameter

Examining behaviour of memory for the working module and module designed by the student as part of the experiment (refer to the circuit diagram):

examining the write behaviour:

- initialization (refer to experiment manual for pin numbers):
  - select=1
  - R/W'=0
- Loading data in the memory (refer to procedure tab for further detail and experiment manual for pin numbers):
  - input(i/p)=1

examining the read behaviour:

- initialization (refer to experiment manual for pin numbers):
  - select=1

    - R/W'=1
- check output:
    - output(o/p)=1
    - it will give the value which was previously written

- color configuration of wire for 5 valued logic supported by the simulator:

    - if value is UNKNOWN, wire color= maroon
    - if value is TRUE, wire color= blue
    - if value is FALSE, wire color= black
    - if value is HI IMPEDENCE, wire color= green
    - if value is INVALID, wire color= orange

the single bit RAM cell can be used to design large memory

- refer to the theory and circuit diagram for designing 4X3 RAM
- the behaviour can be checked as above mentioned procedure

Test plan:

1. Do some read operation by properly setting the R/W', memory enable then give input and check the output.
2. Do some write operation by properly setting the R/W', memory enable then give input and check the output.
3. Do some read operation without setting the memory enable but properly setting the R/W' then give input and check the output.

Use Display units for checking output. Try to use minimum number of components to build. The pin configuration of the canned components are shown when mouse hovered over a component.

Assignment Statements :

1. Design a binary RAM cell using a S-R flipflop, AND gates, NOT gates having select, read/write, input, output and test it by giving proper input.
2. Design a 4X3 RAM memory which will have 4 words each of 3 bits using binary RAM cells, decoder with enable, OR gates and test it by giving proper input.